Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A device comprising:

a decoder control circuit for controlling an MPEG decoder, structured to decode several coded images from ~~more than one~~ at least two MPEG ~~stream~~ streams simultaneously in a plurality of periods, the decoder control circuit receiving, at a beginning of each period, an order to decode a plurality of images of a first or of a second type, the images of the second type being decodable at any time during the period following their decoding command, and the images of the first type being decodable at any time during the two periods following their decoding command, including a priority assignment circuit structured to, at each period, grant among the images a decoding priority to any of the images of the first type that still have not been decoded one period after their decoding order, otherwise, if there are any, to the images of the second type.

2. (Original) The device according to claim 1, wherein the decoder control circuit further includes a pointer memory for storing the beginning addresses of each of the images to be displayed.

3. (Original) The device according to claim 1, wherein said decoder control circuit further includes a safety circuit for adding a predetermined header before each image provided to the decoder so that two images put end to end cannot form a code that causes a malfunction of the decoder.

4. (Original) The device according to claim 3, wherein the device includes the MPEG decoder, and the MPEG decoder is connected to the decoder control circuit.

5. (Original) The device according to claim 1, further comprising:

a memory that stores coded data and decoded data;

a first bus that connects the decoder control circuit to the memory;

a display control circuit connected between a screen and the first bus; and

a microprocessor connected by a second bus to the decoder control circuit and the display control circuit.

6. (Original) The device according to claim 1, wherein the images of the first type are interlaced complete images, and the images of the second type are interlaced half-images.

7. (Original) The device according to claim 1, wherein the images of the first type are interlaced complete images, and the images of the second type are interlaced half-images or non-interlaced complete images.

8. (Previously Presented) A method for prioritizing MPEG images to be decoded, comprising:

receiving first and second image sequences of coded images from more than one MPEG stream, each coded image having an image type that is one of a plurality of image types;

receiving a stream of decoding commands in a series of synchronizing periods, each decoding command corresponding to a respective one of the coded images;

adding each decoding command to a priority list;

prioritizing the decoding commands by assigning to each decoding command a priority level based on the image type of the coded image corresponding to the decoding command;

decoding the coded images in a priority order based on the priorities assigned to the coded images, thereby producing first and second images sequences of decoded images; and

displaying the first and second image sequences.

9. (Original) The method according to claim 8 wherein the plurality of image types includes first and second images types and prioritizing the decoding commands comprises:

assigning a higher priority to a first decoding command corresponding to a coded image of the first image type than to a second decoding command corresponding to a coded image of the second image type if the second decoding command has been on the list for less than one synchronizing period and otherwise assigning a higher priority to the second decoding command than to the first decoding command.

10. (Previously Presented) A method for decoding a plurality of MPEG sequences from more than one MPEG stream simultaneously using a single MPEG decoder, the method comprising:

receiving first and second image sequences of coded images;

receiving a stream of decoding commands, each decoding command corresponding to a respective one of the coded images;

prioritizing the received coded images;

decoding the coded images using the single MPEG decoder, thereby producing decoded images of first and second images sequences; and

saving the decoded images.

11. (Original) The method according to claim 10 wherein the decoding commands are received in a series of synchronizing periods and prioritizing the coded images includes, during each synchronizing period, prioritizing the decoding commands received in the synchronizing period.

12. (Original) The method according to claim 11 wherein prioritizing the coded images includes, during each synchronizing period, assigning a lower priority to the decoding command received during the synchronizing period than to any decoding command received in a prior synchronizing period.

13. (Original) The method according to claim 11 wherein the coded images include first and second sets of coded images and wherein the coded images of the first set are decoded during the synchronizing period in which the decoding commands corresponding to the coded images of the first set are received and the coded images of the second set are decoded during a synchronizing period subsequent to the synchronizing period in which the decoding commands corresponding to the coded images of the second set are received.

14. (Original) The method according to claim 11 wherein the coded images include a first coded image of a first image type and second coded image of a second image type, wherein prioritizing the coded images includes:

assigning a higher priority to the first coded image than to the second coded image if the decoding command corresponding to the first coded image was received in a synchronizing period prior to the synchronizing period in which the decoding command corresponding to the second coded image was received.

15. (Original) The method according to claim 14 wherein the first image type is an interlaced complete image.

16. (Original) The method according to claim 14, wherein said second type of image is an interlaced half image or a non-interlaced complete image.

17. (Original) The method according to claim 10 wherein the coded images are read from a memory device and the decoded images are saved to the memory device.

18. (Previously Presented) A device, comprising:

an MPEG decoder configured to decode a plurality of MPEG image sequences from more than one MPEG stream in parallel; and

a controller coupled to the MPEG decoder and configured to control the MPEG decoder such that:

a received image sequence of a first type is decodable during two periods following an associated decoding order; and

a received image sequence of a second type is decodable during a first period following an associated decoding order.

19. (Previously Presented) The device of claim 18 wherein the controller comprises a prioritizing module configured to assign a decoding priority to received image sequences of the first type that are not decoded in a first period following their associated decoding order.

20. (Previously Presented) The device of claim 18, wherein the controller comprises a pointer memory to store images sequences to be decoded and associated decoding parameters and the controller assigns a decoding priority to received image sequences based at least in part on the associated decoding parameters.

21. (Previously Presented) The device of claim 18 wherein the received image sequences of the first type are interlaced complete-image sequences and the received image sequences of the second type are interlaced half-image sequences.

22. (Previously Presented) The device of claim 18 wherein the controller comprises a prioritizing module configured to assign a first decoding priority to received image sequences of the first type during a second period following their associated decoding order, a second decoding priority to received image sequence of the second type and a third decoding priority to received image sequence of the first type during a first period following their associated decoding order.

23. (Previously Presented) The device of claim 18 wherein the controller comprises means for assigning a decoding priority to received image sequences.

24. (Previously Presented) The device of claim 18 wherein the controller is further configured to control the MPEG decoder such that a first decoded image sequence of a coded image from a first MPEG stream is produced and a second decoded image sequence of a coded image from a second MPEG stream is produced.

25. (Previously Presented) The device of claim 1 wherein the decoder control circuit is further configured to control the MPEG decoder such that a first decoded image sequence of a coded image from a first MPEG stream is produced and a second decoded image sequence of a coded image from a second MPEG stream is produced.

26. (Previously Presented) The method of claim 8 wherein the first decoded image sequence is a decoded image sequence from a first MPEG stream and the second decoded image sequence is a decoded image sequence a second MPEG stream.

27. (Previously Presented) The method of claim 10 wherein the first decoded image sequence is a decoded image sequence from a first MPEG stream and the second decoded image sequence is a decoded image sequence a second MPEG stream.